(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 065 701 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
03.01.2001 Bulletin 2001/01

(51) Int. Cl.[7]: H01L 21/00, C23C 16/00

(21) Application number: 00113952.6

(22) Date of filing: 30.06.2000

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 01.07.1999 US 346646

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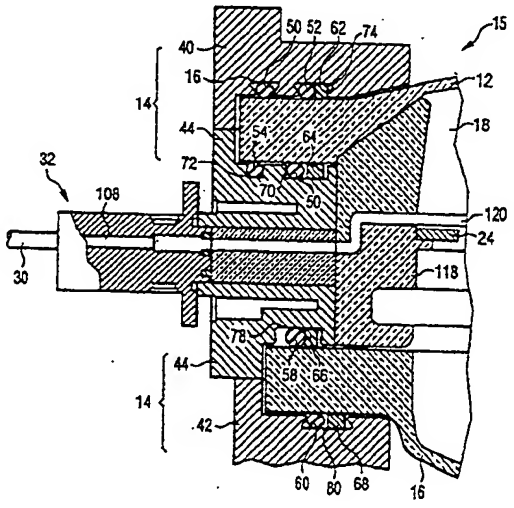
(54) Inert barrier for high purity epitaxial deposition systems

(57) The present invention is an improved semiconductor substrate processing apparatus which includes a processing chamber having a first member, a second member and a processing region; a vacuum tight seal between said first and said second members that enables a pressure controlled environment within said processing region; and a barrier between said first and second members which separates said seal from said processing region, said barrier being substantially non-reactive with processes conducted in said processing region.

FIG 3



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with either or both of the reactant or dopant gases. In this process, the crystallographic nature of the deposited silicon depends upon the temperature of deposition. At low reaction temperatures of about 600°C the deposited silicon is mostly amorphous; when higher deposition temperatures of about 650°C to 800°C are employed, a mixture of amorphous silicon and polysilicon or polysilicon alone will be deposited.

[0009] Processing region 18 could be cleaned after each deposition sequence or after a series of deposition sequences has been conducted. In a typical HCl based periodic cleaning cycle, a chamber clean cycle is conducted for every 10 to 20 μm of silicon deposited in reactor 10. The cleaning cycle is conducted after removing the last wafer of the sequence from chamber 10. Without a wafer present in the chamber, the susceptor temperature is raised to about 1200° C while a mixture of HCl and H_2 is provided to processing region 18. The HCl breaks down the silicon deposits formed within processing region 18 into volatile by-products that are exhausted from processing region 18 via evacuation port 36.

[0010] One problem with current CVD reactors is that O-rings 50, 52, 54, 56, 58 and 60 are degraded by prolonged exposure to the chemistry, temperatures and pressures employed within processing region 18 during the deposition and cleaning processes. Typical removal rates form the HCl cleaning process above are about 2 μm/min. Longer deposition sequences, such as those having about 20μm depositions between cleans, provide higher throughput but increase the length of exposure to HCl and 1200°C which in turn increases the likelihood of O-ring degradation and failure. Degraded or failed O-rings result in contamination of processing region 18 and films formed therein as well as loss of process environment control such as loss of pressure control.

[0011] One measure of the lack of contamination or level of purity within processing region 18 is the resistivity measurement of an undoped epitaxial silicon film deposited in region 18. Since silicon has an intrinsically high resistivity on the order of greater than 800 Ω-cm, resistivity measurements below 800 Ω-cm indicate contamination of some kind within the processing region. A high degree of purity within region 18 is desired initially so that dopants can be incorporated with greater certainty to provide doped silicon films with specific resistivity. O-rings, such as those utilized as in Figures 1 and 2, are typically limited to about 20μm deposition cycles or cleaning cycles of HCl at 1200°C lasting less than about 30 minutes. Because of their direct exposure to region 18, degradation or failure of these O-rings (56 and 58) leads to processing area contamination which in turn results in resistivities on the order of 20-30 Ω-cm.

[0012] What is needed is a processing apparatus which can overcome the shortcomings of the prior art by extending the processing throughput capability of an O-ring sealed reactor beyond 20μm deposition between cleans. Such a reactor would be capable of extended high temperature epitaxial deposition cycles capable of depositing films about 20μm or more thick. Such a reactor would extend the duration of HCl cleans while also preventing O-ring based contamination from reaching the processing region.

[0013] An aspect of the present invention is an improved semiconductor substrate processing apparatus having a processing chamber having a first member, a second member and a processing region; a vacuum tight seal between said first and said second members that enables a pressure controlled environment within said processing region; and a barrier disposed between said first and second members which separates said seal from said processing region, said barrier being substantially non-reactive with processes conducted in said processing region.

[0014] Another aspect of the present invention is an improved apparatus for depositing silicon which includes a processing chamber having a first element, a second element and a processing region; an O-ring between said first and second elements that enables pressure controlled processes within said processing region; and a linearly shaped material comprising expanded polytetrafluoroethylene said material being substantially inert to the temperature, pressure and chemical environment within said processing region, said material having a first notched end, a second notched end adaptively coupled to said first notched end, a thickness and a length wherein said linear material circumscribes said processing region when said first notched end is coupled to said second notched end thereby said inert material separates said processing region from said O-ring.

[0015] Another aspect of the present invention is an improved apparatus for depositing silicon which includes a processing chamber having a top dome, a bottom dome, a base ring and a clamp ring coupled to and separating said top dome and said bottom dome wherein said top dome, bottom dome, base ring and clamp ring define a processing region, a susceptor disposed within said processing region, a plurality of lamps which illuminate said susceptor, and a quartz liner disposed adjacent to said susceptor; a seal disposed between said base ring and each of said domes and a seal between said clamp ring and each of said domes wherein said domes, said base ring and said clamp rings are compressably in contact with said seals to enable a pressure controlled environment within said processing region; and barriers disposed between each of said seals and said processing region wherein said barrier is prevents contaminants from said seals from reaching said processing region, wherein said seals and said barriers are disposed within grooves formed in said clamp ring and said base ring.

[0016] A preferred embodiment of the invention is claimed in the main claim, whereas further preferred embodiments of the invention and the features thereof

where from about 10 Torr to 1000 Torr. Typical pressures are 760 Torr for atmospheric pressure processes and between about 20 Torr to 100 Torr for reduced pressure processes.

[0024] O-rings 50, 52. 54 and 60 are used to evenly distribute the compressive and loading forces of clamp rings and base rings across upper and lower domes 12 and 16. O-rings 50, 52, 54 and 60 also act as secondary pressure seals for processing region 18. Thus, all sealing and loading forces are borne by O-rings 50, 52, 54, 56, 58 and 60. Also illustrated in the representative double dome reactor embodiment of the present invention are the separate grooves formed within upper and lower clamp rings 40 and 42 and base ring 44 to accommodate the O-rings and barrier material of the present invention. Base ring 44 provides separated support O-rings and sealing O-rings such as groove 70 that accommodates primary seal O-ring 56 and barrier 64 while groove 72 accommodates support and secondary seal O-ring 54. Base ring 44 also provides a combined sealing and support O-ring as found in groove 78 that accommodates support and secondary seal O-ring 58 and barrier 66. Upper clamp ring 40 is illustrative of a separate support and sealing O-ring design that includes a groove 76 that accommodates support and sealing O-ring 50 and groove 74 that accommodates a primary sealing O-ring 52 and a barrier 62. Lower clamp ring 42 is illustrative of a combined sealing and support O-ring that includes a single groove 80 that accommodates sealing and support O-ring 60 and a barrier 68. The O-ring and barrier locations and groove configurations illustrated in the embodiment of Figure 3 are merely representative of an O-ring and barrier locations and groove design configuration. One of ordinary skill will appreciate that a wide variety of O-ring and barrier locations and groove size designs may be employed without departing from the spirit of the present invention. Those alternative designs and configurations will vary according to the size and type of reactor into which the barrier of the present invention is to be employed.

[0025] Although under compressive force, inert barriers 62, 64, 66 and 68 are not considered part of the loading, distribution or support for upper and lower domes 12 and 16. Additionally, inert barriers 62, 64, 66 and 68 are not relied on to provide a pressure seal for processing region 18. In fact, tests conducted in a processing reactor similar to reactor 15 that used barriers 62, 64, 66 and 68 alone (i.e., without any O-rings) was unable to provide a sufficient seal for which adequate pressure control could be maintained within processing region 18. Since inert barrier material 62, 64, 66 and 68 alone is inadequate for sealing semiconductor processing reactors, the pressure seal for processing region 18 is provided by the sealing and support O-rings disposed between upper and lower domes 12 and 16 under compressive force of clamp rings 40 and 42 and base ring 44.

[0026] Inert barriers 62, 64, 66 and 68 provide insulation to O-rings from convection heat generated within processing region 18. One reason for positioning a barrier between processing region 18 and an O-ring is that hot gases from processing region 18 would contact only the barrier and not the adjacent O-ring. O-rings still receive considerable thermal energy from the radiation from lamps 28 transmitted through domes 12 and 16 as well as conductive heating from the stainless steel components of side wall 14. Additionally, because gaps exist between quartz domes 12 and 16 and insert 118, inert barriers 64 and 66 are in contact with deposition and cleaning gases used within processing region 18. Because inert barriers 64 and 66 have formed effective barriers between base ring 44 and top and bottom domes 12 and 16, O-rings 58, 54 and 56 are not exposed to the high temperature epitaxial silicon deposition chemistry used during deposition processes and, more importantly, not exposed to the high temperature HCl based chemistry used during cleaning processes.

[0027] The material used for inert barrier 62, 64, 66 and 68 should be substantially non-reactive or inert to the chemistry, temperature, and pressures utilized within processing region 18. Such a material would be capable of sustained exposure to susceptor temperatures ranging between 950°C to 1250°C and reactive source gases typically employed during epitaxial silicon deposition. Additionally, such a material would be capable of prolonged exposure to 1200°C susceptor temperature, and HCl based cleaning chemistry. Such a material would withstand prolonged exposure to both the epitaxial silicon deposition and cleaning cycles without degradation or contaminate generation. Typically in a chamber 15 of Figure 3, a susceptor temperature of 1200°C results in temperatures of between about 280°C to 480°C in the vicinity of barrier materials 62, 64, 66 and 68. Additionally, the barrier material should be so positioned relative to any pathway between an O-ring and processing region 18 such that O-ring contaminates would not reach processing region 18. For example, barrier 64 is positioned so as to block the path from O-rings 54 and 56 to the gap between top dome 12 and quartz insert 118 and on into processing region 18.

[0028] A material with superior heat and chemical resistant properties suitable for use as a barrier material is polytetrafluoroetheylene (PTFE). The PTFE may be produced in an expanded porous form as taught in U.S. Patent 3,953, 566 issued April 27, 1976 to Gore. Suitable barrier materials may also be produced with limited long term creep by wrapping a core of elongated or expanded PTFE with a high strength film of expanded PTFE as discussed in U.S. Patent 5,494,301 and U.S. Patent 5,492,336 both of which are assigned to W.L. Gore Associates. One material suitable as a barrier material is an expanded polytetrafluoroethylene with high multidirectional tensile strength such as that available from W.L. Gore Associates under the product name Gore BG.

[0029] Figure 4 illustrates an expanded PTFE bar-

upper clamp ring 40. Although illustrated with base ring 44 and upper dome 12, similar procedures and dimensional requirements apply to O-rings 50, 52 and barrier 62 in upper clamp ring 40; O-rings 58 and barrier 66 in the lower surface of base ring 44; and O-ring 60 and barrier 68 in lower clamp ring 42. Barrier 64 is disposed adjacent to O-ring 56 in a groove 70 formed within stainless steel base ring 44. No adhesives are used to bond barrier 64 to either base ring 44 or O-ring 56. More importantly adhesives should not be used since any adhesive would defeat the degree of freedom employed by notched, slideably coupled ends of barrier 64. The slideably coupled ends A and B of barrier 64 are intended move freely along the circumference of processing region 18 within groove 70 to compensate for shrinkage of barrier 64 along its length and ensure adequate separation between the adjacent O-ring and processing region 18. Additional grooves are provided to accommodate other loading and sealing O-rings and barriers. For example, support and sealing O-ring 54 is disposed in groove 72 and O-ring 56 is disposed adjacent to barrier 64 in groove 70. Grooves 72 and 70 are formed in base ring 44.

[0037] Groove 70 has a depth (d) compatible with the size of reactor 15, the overall thickness of base ring 44, the cross-sectional diameter of O-rings 54, 56. Once the groove depth is determined, the original or unloaded thickness t of the barrier is selected to ensure sufficient contact between the top and bottom barrier surfaces and the members between which the barrier is positioned. The barrier material loading conditions provide sufficient compression to ensure the barrier separates the O-ring from the processing region. The original or unloaded thickness t also compensates for barrier shrinkage occurring in the t dimension. The thickness t is selected such that when shrinkage occurs in the t dimension, the barrier material still fills the allotted space between the members with sufficient contact to provide an effective barrier. As a result, to the degree that the barrier material shrinks in the t direction, the barrier remains intact and separates the adjacent O-ring from the processing region.

[0038] In a representative embodiment where reactor 15 is a CVD double dome reactor capable of processing 300mm diameter workpieces and barrier 64 has an unloaded thickness (t) of 0.285 inches, groove 70 has a depth of about 0.215 inches. A suitable barrier material would have an initial, unloaded thickness on the order of 1.3 to 1.5 times the depth of the groove 70 to which it will be installed. Thus, the representative embodiment of Figure 9 illustrates a groove depth of 0.215 inches and an initial barrier thickness of 0.285 which results in a barrier about 1.32 times as thick as the depth of its associated groove. Additional grooves are formed in top clamp 40, base ring 44 and bottom clamp 42 in order to similarly situate O-rings 50, 52, 54, 58 and 60 and barrier materials 62, 66 and 68.

[0039] In the loaded condition illustrated in Figure 10, upper clamp ring 40 and base ring 44 provide compressive force to O-rings 50, 52, 54 and 56 in order to support top dome 12. In the loaded condition of Figure 10, spacing 75 is maintained between stainless steel base ring 44 and top quartz dome 12. In the representative embodiment of Figure 10, spacing 75 is on the order of 0.02 inches. A similar spacing exists between upper clamp ring 40 and top dome 12. Although not shown in Figure 10, spacings exist between bottom dome 16 and both base ring 44 and lower clamp ring 42. As a result of compressive loading between clamp ring 40 and base ring 44, upper dome 12 is supported by O-rings 50, 52, 54 and 56. Although not used to enable a pressure seal for processing region 18, barriers 62 and 64 are also compressed from their original thickness. For example, the barrier 64 of Figure 10 is about 0.235 inches thick from an original unloaded thickness of about 0.285 inches. This represents a slight compressive force. Although insufficient for sealing, this force is sufficient to ensure complete enough contact along the width of barrier 64 between top dome 12 and base ring 44 via groove 70 to ensure an effective barrier is formed between O-ring 56 and processing region 18.

[0040] Processing chambers employing the barrier layer of the present invention have demonstrated higher throughput and improved processing windows. For example, prior art systems which utilized O-rings only (i.e. chamber 10) were limited to three consecutive 20 μm deposition cycles followed by a single 1200°C HCl clean lasting approximately 30 minutes. Additionally, the resistivity of epitaxial silicon produced in prior art reactors after conducting the above deposition and cleaning sequence is on the order of 20-30 Ω-cm. Generally, intrinsic silicon resistively below 200 Ω-cm is unacceptable for most commercial epitaxial silicon process requirements. Such a low resistivity in this case in indicative of O-ring degradation, and possible failure or other contamination within processing region 18.

[0041] Turning now to Figures 11, 12 and 13, the insulating and contaminate preventing properties of a processing reactor utilizing the barrier layer of the present invention can be better appreciated. Figure 11 illustrates a stress test conducted in a reactor 15 to evaluate the improved insulating properties of the barrier material of the present invention. The graph represents a temperature reading taken at O-ring 56 located adjacent to barrier material 64 and separated from processing region 18. The test included six consecutive epitaxial silicon deposition processes up to approximately time 2600, followed by an extended 1200°C HCl clean which lasted from about time 2600 to about 4600, or approximately 33 minutes. This extended HCl clean was immediately followed by an additional six epitaxial silicon deposition cycles. As indicated by the graph, an O-ring used in conjunction with a barrier material of the present invention was exposed to a maximum temperature of about 235°C which occurred after the prolonged 1200°C clean.

some reactor designs, the backsides of susceptor 22 and preheat ring 24. During the deposition cycle, barrier 64 prevents the heated deposition reactants within processing region 18 that enter the gap between liner 118 and top dome 12 from reaching O-ring 56. Similarly, barrier 66 prevents heated deposition reactants within processing region 18 that enter the gap between liner 118 and bottom dome 16 from reaching O-ring 58. Barriers 62, 64, 66 and 68 also provide thermal insulation from the high temperatures that exist in processing region 18 during epitaxial silicon deposition.

[0050] Additionally, because the barriers 64 and 66 are advantageously located between the O-rings and processing region 18 particles or other contaminants generated by the O-rings are prevented from entering processing region 18 and contaminating the film deposited on substrate 20. Likewise, barrier 62 would prevent particles or contaminants generated by O-rings 50 and 52 from reaching and potentially coating or otherwise adversely impacting the transmission of radiant energy from lamps 26 in the top portion of reactor 15 into processing region 18. Similarly, barrier 68 would prevent particles or contaminants generated by O-ring 60 from reaching and potentially coating or otherwise adversely impacting the transmission of radiant energy from lamps 26 in the bottom portion of reactor 15 into processing region 18.

[0051] The deposition cycle is repeated for each substrate to be processed. In a typical epitaxial deposition sequence, a number of substrates will be processed and then a single clean sequence will be performed inside processing region 18 to remove deposits accumulated during the deposition cycle. Particularly contemplated is a commercially viable deposition and clean sequence wherein about 20μm of epitaxial silicon deposition is followed by a single, prolonged, HCl based cleaning cycle lasting up to between about 5 to 10 minutes. After the last substrate of the deposition sequence has been processed and removed from the processing region, the temperature of processing region 18, measured at susceptor 22, is raised to about 1200°C. Next, HCl is introduced into processing region 18 via inlet 32. The gaseous HCl dissociates within processing region 18 and reacts with the silicon deposits and other accumulations to form volatile by-products. These volatile by-products are subsequently exhausted from processing region 18 via exhaust port 36.

[0052] As with the deposition process, barriers 64 and 66 protect sealing O-rings 56 and 58 from degradation as a result of direct contact with the high temperature gases employed during the cleaning process. Particularly with regard to the cleaning process, barriers 64 and 66 prevent chemical attack that would result from contact between O-rings 56 and 58 and the reactive cleaning agents employed within processing region 18 during the cleaning cycle. In the 1200°C HCl clean typical to epitaxial reactors, one highly reactive cleaning agent employed is chlorine.

[0053] During the cleaning cycle, barrier 64 prevents the heated cleaning gases within processing region 18 that enter the gap between liner 118 and top dome 12 from reaching O-ring 56. Similarly, barrier 66 prevents heated cleaning gases within processing region 18 that enter the gap between liner 118 and bottom dome 16 from reaching O-ring 58. Barriers 62, 64, 66 and 68 also provide thermal insulation from the high HCl clean temperatures employed in processing region 18.

[0054] Additionally, because the barriers 64 and 66 are advantageously located between the O-rings and processing region 18 particles or other contaminants generated by the O-rings are prevented from entering processing region 18 and interfering with the cleaning process. If O-rings 50 and 52 become degraded and produce particles or contaminants then barrier 62 would prevent those particles or contaminants from reaching and potentially coating or otherwise adversely impacting the transmission of radiant energy from lamps 26 in the top portion of reactor 15 into processing region 18. If O-ring 60 becomes degraded and produces particles or contaminants, then barrier 68 would prevent those particles or contaminants from reaching and potentially coating or otherwise adversely impacting the transmission of radiant energy from lamps 26 in the bottom portion of reactor 15 into processing region 18.

[0055] Although described with regard to epitaxial silicon deposition, other processing operations could advantageously utilize the barrier layer of the present invention. For example, amorphous silicon, doped silicon and polysilicon deposition processes employ a 1200°C HCl clean cycle similar to the one described above. These types of deposition reactors could employ the barrier of the present invention to likewise achieve the ability to conduct prolonged 1200°C HCl clean cycles without O-ring degradation. Just as the barrier of the present invention prevents chloride chemical attack, the barrier could be employed with other clean chemistries to likewise prevent other types of chemical attack as well. For example, the barrier of the present invention could be employed to prevent fluorine chemical attack in those processing chambers that employ fluorine based clean chemistries such as the use of NF_3.

Claims

1. A semiconductor substrate processing apparatus comprising:

   (a) a processing chamber having a first member, a second member and a processing region;

   (b) a vacuum tight seal between said first and said second members that enables a pressure controlled environment within said processing region; and

which illuminate said susceptor, and a quartz liner disposed adjacent to said susceptor;

(b) a seal disposed between said base ring and each of said domes and a seal between said clamp ring and each of said domes wherein said domes, said base ring and said clamp rings are compressably in contact with said seals to enable a pressure controlled environment within said processing region ; and

(c) barriers disposed between each of said seals and said processing region wherein said barrier is prevents contaminants from said seals from reaching said processing region.

wherein said seals and said barriers are disposed within grooves formed in said clamp ring and said base ring.

15. An apparatus according to claim 14 wherein said base ring and said clamp ring are formed from stainless steel.

16. An apparatus according to claim 14 wherein said seals have circular cross sections and said barriers have rectangular cross sections.

17. An apparatus according to claim 14 wherein the thickness of said barriers is less than twice the depth of said grooves.

FIG 2

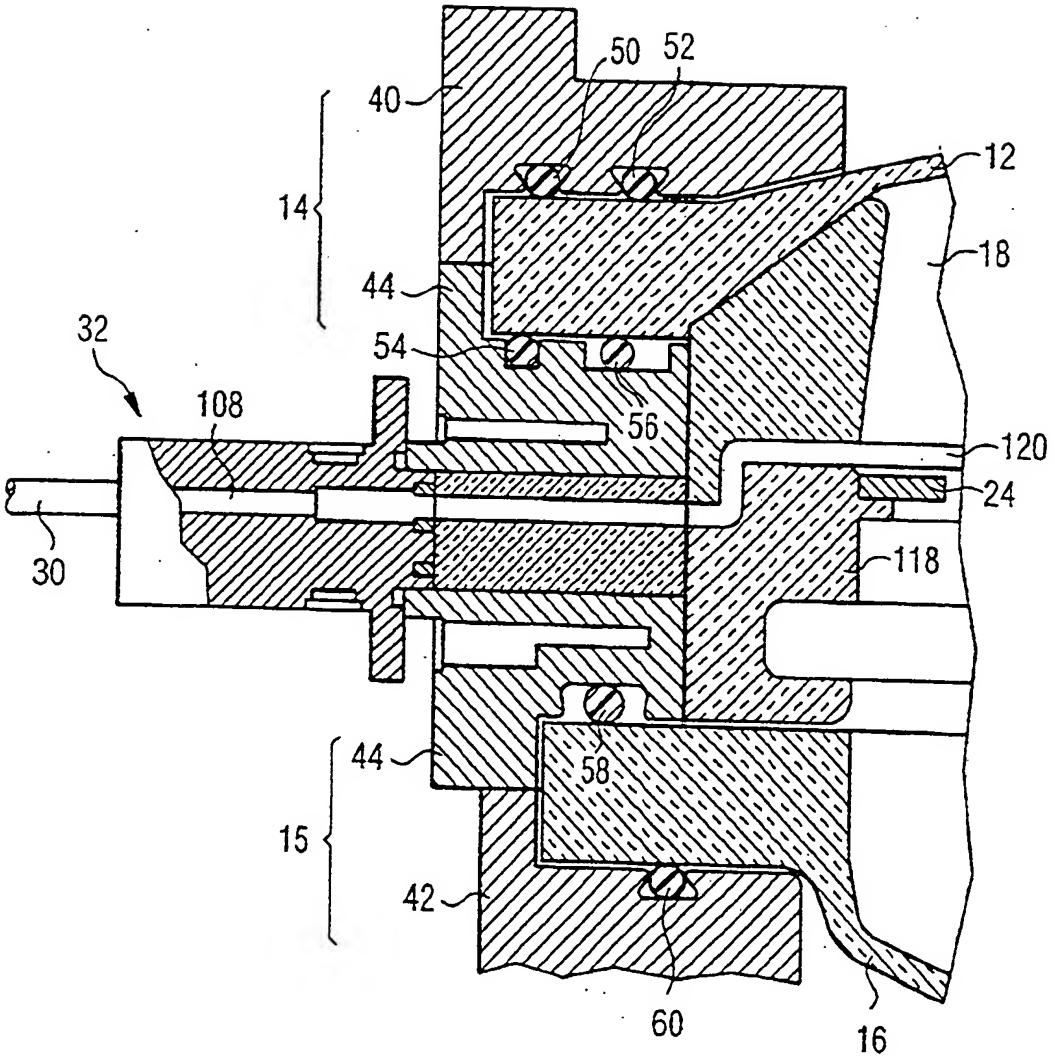


FIG 4

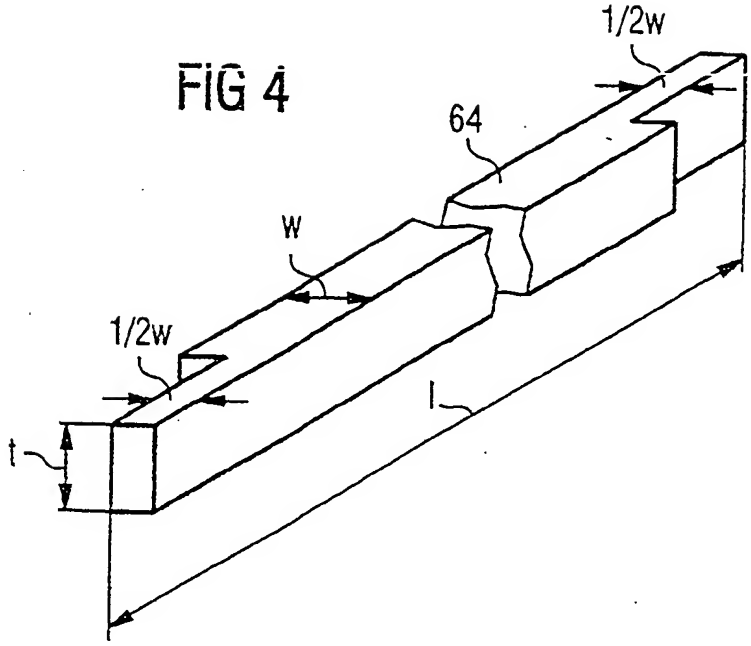


FIG 5

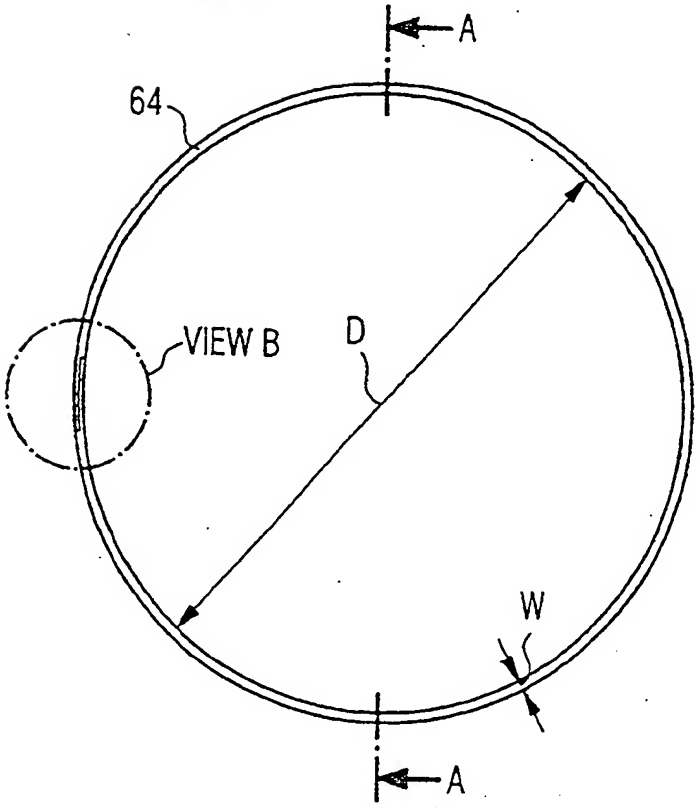


FIG 6
VIEW A-A

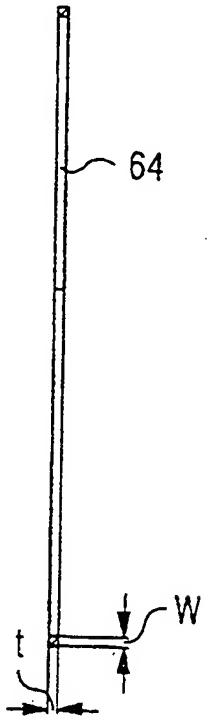


FIG 9

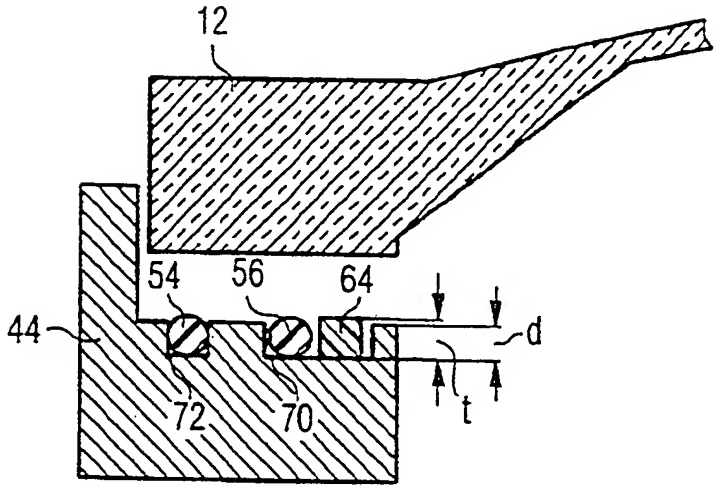


FIG 10

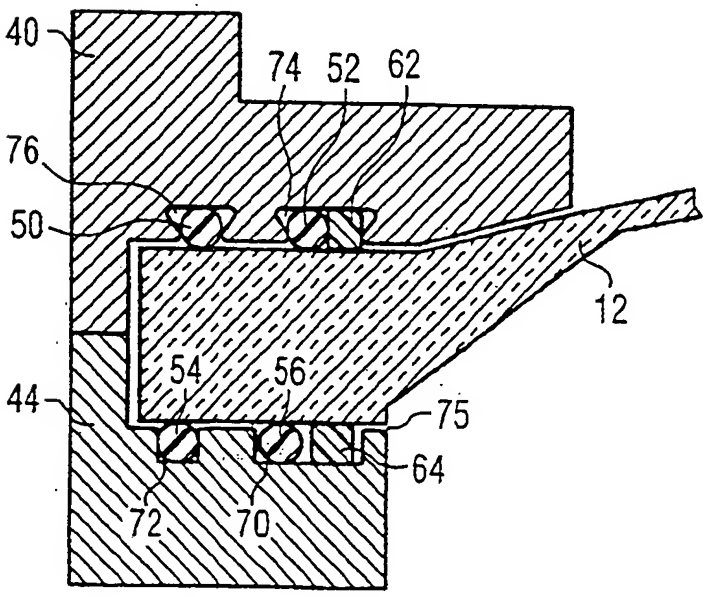
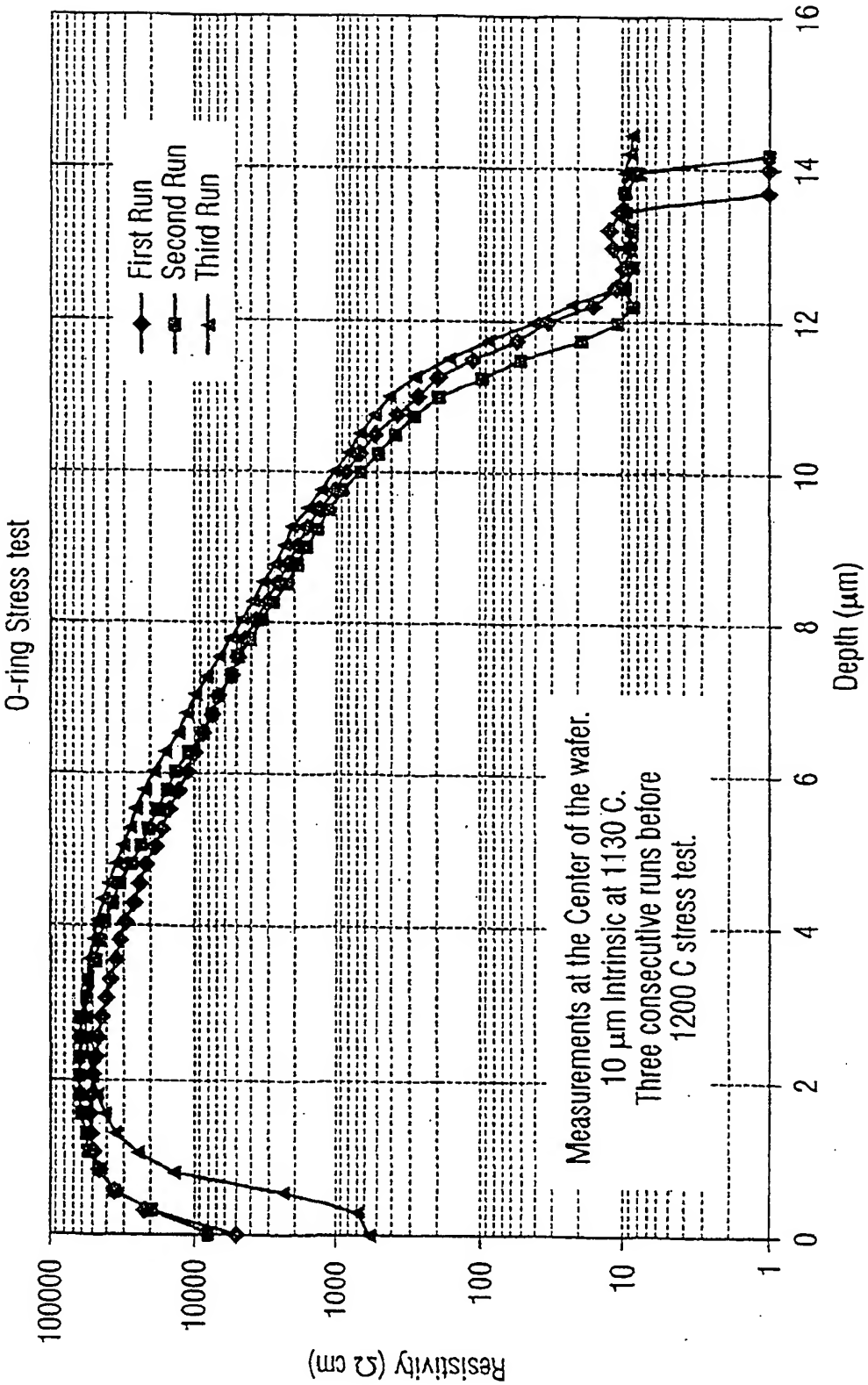


FIG 12


O-ring Stress test
First Run
Second Run
Third Run
Measurements at the Center of the wafer.
10 µm Intrinsic at 1130 C.
Three consecutive runs before
1200 C stress test.
Resistivity (Ω cm)
100000
10000
1000
100
10
1
0
2
4
6
8
10
12
14
16
Depth (µm)

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 065 701 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
11.07.2001 Bulletin 2001/28

(43) Date of publication A2:
03.01.2001 Bulletin 2001/01

(21) Application number: **00113952.6**

(22) Date of filing: **30.06.2000**

(51) Int Cl.7: **H01L 21/00**, C23C 16/00, C23C 16/44

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **01.07.1999 US 346646**

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(54) Inert barrier for high purity epitaxial deposition systems

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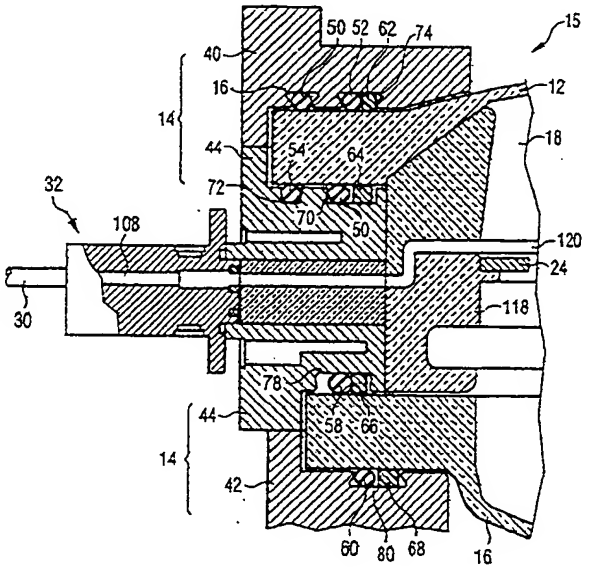
FIG 3



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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 11 3952

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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21-05-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5534073 A	09-07-1996	JP 6244269 A	02-09-1994
		KR 183466 B	15-04-1999
		US 5976260 A	02-11-1999
US 5914050 A	22-06-1999	EP 1017877 A	12-07-2000
		WO 9915712 A	01-04-1999
US 5492336 A	20-02-1996	US 5486010 A	23-01-1996
		US 5494301 A	27-02-1996
		US 5551706 A	03-09-1996
		AU 5407494 A	27-03-1995
		CA 2169749 A	16-03-1995
		EP 0717820 A	26-06-1996
		JP 9502512 T	11-03-1997
		WO 9507422 A	16-03-1995
		CA 2157283 A	27-10-1994
		DE 69312745 D	04-09-1997
		DE 69312745 T	04-12-1997
		EP 0695405 A	07-02-1996
		JP 8509052 T	24-09-1996
		WO 9424467 A	27-10-1994
US 5788799 A	04-08-1998	JP 10070112 A	10-03-1998
US 5494301 A	27-02-1996	CA 2157283 A	27-10-1994
		DE 69312745 D	04-09-1997
		DE 69312745 T	04-12-1997
		EP 0695405 A	07-02-1996
		JP 8509052 T	24-09-1996
		WO 9424467 A	27-10-1994
		US 5486010 A	23-01-1996
		US 5492336 A	20-02-1996
		US 5551706 A	03-09-1996